REMARKS

The Office Action dated February 23, 2006, has been received and carefully considered. In this response, claims 1, 3, 5-7, 9-12, 14, and 15 have been amended. Entry of the amendments to claims 1, 3, 5-7, 9-12, 14, and 15 is respectfully requested. Reconsideration of the outstanding rejections in the present application is also respectfully requested based on the following remarks.

I. THE RESTRICTION REQUIREMENT

On page 1 of the Office Action, the election/restriction requirement was made final. However, as set forth in Applicants' response filed January 5, 2006, it is respectfully submitted that the Examiner has failed to explain how the invention defined by claims 1-10 is independent from the invention defined by claims 11-15. Indeed, the Examiner acknowledges that the invention defined by claims 1-10 is related to the invention defined by claims 11-15, and vice versa. Thus, the invention defined by claims 1-10 and the invention defined by claims 11-15 are related and are not independent from each other. Accordingly, it is respectfully submitted that the election/restriction requirement is improper,

and the withdrawal of such election/restriction requirement is respectfully requested.

II. THE OBVIOUSNESS REJECTION OF CLAIMS 1-10

On pages 2-4 of the Office Action, claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ball et al. (U.S. Patent No. 6,246,112). This rejection is hereby respectfully traversed with amendment.

As stated in MPEP § 2143, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Also, as stated in MPEP § 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion,

or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Further, as stated in MPEP § 2143.03, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). That is, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970). Additionally, as stated in MPEP § 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). Finally, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Regarding claim 1, the Examiner asserts that Ball et al. teaches the claimed invention. However, it is respectfully submitted that Ball et al. fails to teach, or even suggest, a method for accommodating electronic components on a multilayer signal routing device comprising: determining a component space that is required to accommodate a plurality of electronic components on a surface of a multilayer signal routing device; forming at least one channel on at least the surface of the multilayer signal routing device by not deploying electrically conductive vias in the multilayer signal routing device that extend through at least the surface of the multilayer signal routing device coinciding with a location of the at least one channel, wherein the at least one channel has a channel space that is equal to or greater than the component space; and mounting at least a portion of the plurality of electronic components on the surface of the multilayer signal routing device within the at least one channel, as presently claimed.

Specifically, Ball et al. fails to teach, or even suggest, a method for accommodating electronic components on a multilayer signal routing device, as claimed. In contrast, as the Examiner acknowledges, Ball et al. merely teaches interleaving a plurality of ground traces with a plurality of signal traces. Nowhere does Ball et al. teach how electronic components are

accommodated on a multilayer signal routing device. Indeed, Ball et al. provides no reason to accommodate electronic components on a multilayer signal routing device since Ball et al. does not teach, or even suggest, any need to accommodate electronic components on a multilayer signal routing device.

Also, Ball et al. fails to teach, or even suggest, determining a component space that is required to accommodate a plurality of electronic components on a surface of a multilayer signal routing device, as claimed. Indeed, Ball et al. fails to discuss anything regarding how a component space, that is required to accommodate a plurality of electronic components on a surface of a multilayer signal routing device, is determined. Ball et al. also fails to provide any suggestion or motivation as to how a component space is determined since Ball et al. fails to discuss anything regarding accommodating a plurality of electronic components on a surface of a multilayer signal routing device.

Further, Ball et al. fails to teach, or even suggest, forming at least one channel on at least the surface of the multilayer signal routing device by not deploying electrically conductive vias in the multilayer signal routing device that extend through at least the surface of the multilayer signal routing device coinciding with a location of the at least one

channel, wherein the at least one channel has a channel space that is equal to or greater than the component space, as presently claimed. Indeed, Ball et al. teaches away from the claim element by disclosing that vias 32 extend to the bottom surface of package 38 and to the top surface of package 39 (e.g., see column 4, lines 3-8 and 28-31). Furthermore, Ball et al. does not teach, or even suggest, channels, nor any need for such channels. As shown in Figure 5, Ball et al. simply routes traces 34 in between vias 32, and does not teach, or even suggest, forming at least one channel that has a channel space that is equal to or greater than the component space, as claimed.

Additionally, Ball et al. fails to teach, or even suggest, mounting at least a portion of the plurality of electronic components on the surface of the multilayer signal routing device within the at least one channel, as presently claimed. First of all, as discussed above, Ball et al. does not teach, or even suggest, forming at least one channel that has a channel space that is equal to or greater than the component space, as claimed. Secondly, Ball et al. does not teach, or even suggest, mounting at least a portion of the plurality of electronic components on the surface of the multilayer signal routing device within the at least one channel, as presently claimed.

Indeed, in contrast, Ball et al. shows traces 34 routed in areas between vias 32, and thus there would be nowhere to mount any electronic components in such areas (e.g.,. see Figure 5).

In view of the foregoing, it is respectfully submitted that Ball et al. fails to teach, or even suggest, the recited elements of claim 1. Accordingly, it is respectfully submitted that claim 1 is allowable over Ball et al.

Claims 2-10 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-10 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 1-10 be withdrawn.

III. THE OBVIOUSNESS REJECTION OF CLAIM 1

On pages 4-5 of the Office Action, claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Haller et al. (U.S. Patent No. 5,357,403). This rejection is hereby respectfully traversed with amendment.

Regarding claim 1, the Examiner asserts that Haller et al. teaches the claimed invention. However, it is respectfully submitted that Haller et al. fails to teach, or even suggest, a method for accommodating electronic components on a multilayer signal routing device comprising: determining a component space that is required to accommodate a plurality of electronic components on a surface of a multilayer signal routing device; forming at least one channel on at least the surface of the multilayer signal routing device by not deploying electrically conductive vias in the multilayer signal routing device that extend through at least the surface of the multilayer signal routing device coinciding with a location of the at least one channel, wherein the at least one channel has a channel space that is equal to or greater than the component space; and mounting at least a portion of the plurality of electronic components on the surface of the multilayer signal routing device within the at least one channel, as presently claimed.

Specifically, Haller et al. fails to teach, or even suggest, a method for accommodating electronic components on a multilayer signal routing device, as claimed. In contrast, as the Examiner acknowledges, Haller et al. merely teaches the use of an alignment conductor in a high density interconnect structure. Nowhere does Haller et al. teach how electronic

components are accommodated on a multilayer signal routing device. Indeed, Haller et al. provides no reason to accommodate electronic components on a multilayer signal routing device since Haller et al. does not teach, or even suggest, any need to accommodate electronic components on a multilayer signal routing device.

Also, Haller et al. fails to teach, or even suggest, determining a component space that is required to accommodate a plurality of electronic components on a surface of a multilayer signal routing device, as claimed. Indeed, Haller et al. fails to discuss anything regarding how a component space, that is required to accommodate a plurality of electronic components on a surface of a multilayer signal routing device, is determined. Haller et al. also fails to provide any suggestion or motivation as to how a component space is determined since Haller et al. fails to discuss anything regarding accommodating a plurality of electronic components on a surface of a multilayer signal routing device.

Further, Haller et al. fails to teach, or even suggest, forming at least one channel on at least the surface of the multilayer signal routing device by not deploying electrically conductive vias in the multilayer signal routing device that extend through at least the surface of the multilayer signal

routing device coinciding with a location of the at least one channel, wherein the at least one channel has a channel space that is equal to or greater than the component space, as presently claimed. The Examiner is reminded that, as stated in MPEP § 2143.03, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Haller et al. clearly fails to teach, or even suggest, this claim element.

Additionally, Haller et al. fails to teach, or even suggest, mounting at least a portion of the plurality of electronic components on the surface of the multilayer signal routing device within the at least one channel, as presently claimed. First of all, as discussed above, Haller et al. does not teach, or even suggest, forming at least one channel that has a channel space that is equal to or greater than the component space, as claimed. Secondly, Haller et al. does not teach, or even suggest, mounting at least a portion of the plurality of electronic components on the surface of the multilayer signal routing device within the at least one channel, as presently claimed. Indeed, Haller et al. does not even discuss mount electronic components in any manner.

In view of the foregoing, it is respectfully submitted that Haller et al. fails to teach, or even suggest, the recited elements of claim 1. Accordingly, it is respectfully submitted that claim 1 is allowable over Haller et al.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 1 be withdrawn.

IV. CONCLUSION

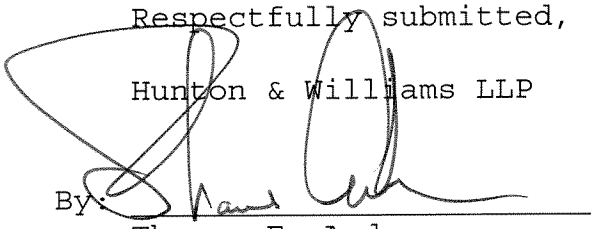
In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

Hunton & Williams LLP



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APPENDIX A

1 (Currently Amended). A method for accommodating electronic components on a multilayer signal routing device, the method comprising the steps of:

determining a component space that is required to accommodate a plurality of electronic components on a surface of a multilayer signal routing device; ~~and~~

forming at least one ~~signal routing~~ channel on at least the surface of the multilayer signal routing device by not deploying electrically conductive vias in the multilayer signal routing device that extend through at least the surface of the multilayer signal routing device coinciding with a location of the at least one channel, the at least one ~~signal routing~~ channel having a channel space that is equal to or greater than the component space; and

mounting at least a portion of the plurality of electronic components on the surface of the multilayer signal routing device within the at least one channel.

2 (Original). The method of claim 1, wherein the step of determining a component space comprises the steps of:

determining a number of the plurality of electronic components that are to be mounted on the surface of the

multilayer signal routing device; and

determining a required space for each of the number of the plurality of electronic components that are to be mounted on the surface of the multilayer signal routing device.

3 (Currently Amended). The method of claim 1, wherein the step of forming at least one ~~signal routing~~ channel comprises the step of:

forming at least two relatively aligned electrically conductive micro-vias in the multilayer signal routing device coinciding with the location of the at least one ~~signal routing~~ channel formed on ~~the~~ a secondary surface of the multilayer signal routing device.

4 (Original). The method of claim 1, wherein the surface of the multilayer signal routing device is a secondary surface of the multilayer signal routing device, wherein a plurality of electrically conductive pads are formed on a primary surface of the multilayer signal routing device opposite the secondary surface of the multilayer signal routing device.

5 (Currently Amended). The method of claim 4, wherein at least two relatively aligned electrically conductive micro-vias are

formed in the multilayer signal routing device in electrical connection with at least two respective ones of the electrically conductive pads and coinciding with the location of the at least one ~~signal routing~~ channel formed on the secondary surface of the multilayer signal routing device.

6 (Currently Amended). The method of claim 5, further comprising the step of:

mounting at least a portion of the plurality of electronic components on the secondary surface of the multilayer signal routing device within the at least one ~~signal routing~~ channel formed on the secondary surface of the multilayer signal routing device.

7 (Currently Amended). The method of claim 5, further comprising the step of:

forming an electrically conductive pad on the secondary surface of the multilayer signal routing device within the at least one ~~signal routing~~ channel formed on the secondary surface of the multilayer signal routing device.

8 (Original). The method of claim 7, further comprising the step of:

forming an electrically conductive trace on the secondary surface of the multilayer signal routing device electrically connected to the electrically conductive pad formed on the secondary surface of the multilayer signal routing device.

9 (Currently Amended). The method of claim 7, further comprising the step of:

mounting at least one of the plurality of electronic components on the secondary surface of the multilayer signal routing device in electrical connection with the electrically conductive pad formed on the secondary surface of the multilayer signal routing device and coinciding with the position of the at least one ~~signal routing~~ channel formed on the secondary surface of the multilayer signal routing device.

10 (Currently Amended). The method of claim 1, wherein the at least one ~~signal routing~~ channel formed on the surface of the multilayer signal routing device has at least one of a vertical, horizontal, and diagonal orientation portion along the surface of the multilayer signal routing device.

11 (Currently Amended). A multilayer signal routing device comprising:

a primary surface having a plurality of electrically conductive pads formed thereon, a group of the plurality of electrically conductive pads in respective electrical connection with a group of electrically conductive micro-vias formed in the multilayer signal routing device; and

a secondary surface having a ~~signal routing~~ channel formed thereon coinciding with the location of the group of electrically conductive micro-vias, the ~~signal routing~~ channel having a channel area on the secondary surface for accommodating an electronic component mounted on the secondary surface.

12 (Currently Amended). The multilayer signal routing device of claim 11, wherein the secondary surface has an electrically conductive pad formed thereon within the ~~signal routing~~ channel.

13 (Original). The multilayer signal routing device of claim 12, wherein the secondary surface has an electrically conductive trace formed thereon, the electrically conductive trace in electrical connection with the electrically conductive pad formed on the secondary surface.

14 (Currently Amended). The multilayer signal routing device of claim 12, wherein the electronic component is mounted on the

secondary surface within the ~~signal routing~~ channel in electrical connection with the electrically conductive pad formed on the secondary surface.

15 (Currently Amended). The multilayer signal routing device of claim 11, wherein the ~~signal routing~~ channel has at least one of a vertical, horizontal, and diagonal orientation portion along the secondary surface of the multilayer signal routing device.